

## CLEAN COPY OF CLAIM 1

1. (Thrice Amended) A method of forming gates in a semiconductor device having a non-linear top profile, the method comprising the steps of:

5 forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device;

depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially;

10 patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer and the dummy gate insulating layer using the mask pattern as an etch barrier, creating a plurality of patterned dummy gate polysilicon and insulating layers each having sidewalls, wherein the patterned dummy gate polysilicon and insulating layers are formed on the semiconductor substrate and on the field oxide layer;

forming spacers at the sidewalls of the patterned dummy gate polysilicon and insulating layers;

15 depositing an insulating interlayer on the resultant structure after forming the spacers;

20 exposing a surface of the patterned dummy gate polysilicon and insulating layers by carrying out an oxide layer chemical mechanical polishing (CMP) process utilizing a first high selection ratio sufficient to polish the insulating ~~layer~~ interlayer but insufficient to polish the patterned dummy gate polysilicon and insulating layers, wherein the first high selection ratio between the insulating interlayer and the dummy gate polysilicon layer is over 20;

forming a damascene structure by removing the patterned dummy gate polysilicon and insulating layers using the insulating interlayer as another etch barrier;

25                    depositing a gate insulating layer and a gate metal layer on the entire surface of  
the semiconductor substrate having the damascene structure; and  
                     exposing a surface of the insulating interlayer by carrying out a metal CMP  
process utilizing a second high selection ratio sufficient to polish the metal layer but  
insufficient to polish the insulating interlayer, wherein the second high selection ratio  
30                    between the insulating interlayer and the gate metal layer is over 50.